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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,263	01/24/2000	Jing Wang		6937

7590 06/16/2003

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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2189	9

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/490,263	WANG ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-17,19-25,27-33,35-42,44-53 and 55-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-17,19-25,27-33,35-42,44-53 and 55-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 14-17, 19-25, 27-32, 38-42, 46-53, 55-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Larky et al. (US Patent 6,389,495)

As per claim 1, Larky discloses USB host system operationally coupled to a computing system with a main processor, comprising:

- a first processor (fig.1, 126) that implements a USB driver without using the main processor (fig.1, 116) resources; (col.4, lines 26-44)
- a downstream USB port; (fig.1, 106)
- a communication area directly accessible by both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, (col.7, lines 21-67)
- wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the first

processor schedules and completes the request via a USB host controller. (col.4, lines 1-44)

As per claim 2, Larky discloses wherein the communication area is a dual port memory. (col.8, lines 51-64)

As per claim 3, Larky discloses wherein the communication area consists of multiple FIFO registers. (col.9, lines 58-61)

As per claim 4, Larky discloses wherein an interrupt polled from a USB interrupt pipe is converted to an interrupt signal to the main processor. (col.9, lines 26-48, wherein decode implies converting)

e. As per claim 5, Larky discloses wherein the processor interfaces with the host system via a standard microprocessor bus. (fig.1, 106)

As per claim 11, Larky discloses a USB host system operationally coupled to a computing system, comprising:

- a first processor (fig. 1, 126) that implements a USB driver without using the main processor (fig.1, 116) resources; (col.2, lines 45-59)
- a downstream USB port; and (fig.1, 106)
- an interface between the first processor and second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system. (col.7, lines 21-37)
- wherein the interface comprises a memory (fig.1, 122) that is directly accessed by both the first and second processors, (col.7, lines 34-53) and

- wherein the second processor interfaces with the host system via a standard microprocessor bus. (fig.1, 106)

As per claim 6, 14, Larky discloses wherein a hub is used to provide multiple downstream USB ports. (fgi.1, 130), (col.5, lines 16-26)

As per claim 7, Larky discloses wherein data in the communication area is directly sent out on a USB bus. (fig.3, 300, col.7, lines 21-33)

As per claim 8, Larky discloses wherein data received from the USB bus are written directly in the communication area. (col.7, lines 1-67)

As per claim 9, Larky discloses wherein the USB host system provides a USB function to the main processor. (col.4, lines 1-14)

As per claim 10, Larky discloses wherein the second processor runs an operating system supporting USB, and the USB host system provides a USB host function to the second processor by intercepting calls to a USB driver in the operating system. (col.6, lines 5-35), (col.7, lines 21-53)

As per claim 15, Larky discloses wherein the host system is used to provide a USB host function to the second processor. (col.7, lines 21-53)

As per claim 16, Larky discloses

- wherein the second processor runs an operating system supporting a USBD, (col.6, lines 17-25)
- wherein the host system provides a USB host function to the second processor, including a USBD function, and (col.6, lines 5-53)

- wherein the host system processes a USB transfer request by the second processor by intercepting calls to the USBD in the operating system and passing the calls to the USBD in the host system. (col.7, lines 21-52), (col.6, lines 5-35)

As per claim 17, Larky discloses an information processing system comprising:

- a first processor; (fig.1, 126)
- a data transfer host system comprising a second processor implementing a first data transfer driver managing a data transfer between the first processor and a device; (col.7, lines 21-53)
- a data transfer port for connecting the device to the data host system; (fig.1, 130) I/O hub implies connection port)
- an interface between the host system and the first processor that provides a high-level view of the data transfer process to the first processor, (col.7, lines 21-37)
- wherein the interface comprises an area in a memory (fig.1, 122) that is directly accessible by both the first processor and the second processor. (col.7, lines 34-53)

As per claim 19, Larky discloses wherein the second processor is used to reduce the number of interrupts to the first processor. (col.7, lines 49-53)

As per claim 20, Larky discloses wherein the second processor is used to reduce the frequency of interrupts to the first processor. (col.7, lines 49-53)

As per claim 21, Larky discloses wherein the first processor interfaces the data transfer host system via a standard microprocessor bus. (fig.1, 106)

As per claim 22, Larky discloses wherein a hub (fig.1, 130) is used to provide multiple ports for connecting a plurality of devices. (col.5, lines 16-26)

As per claim 23, Larky discloses wherein the first processor contains a second data transfer driver capable of managing the data transfer, and wherein a data transfer request by the first processor to the second data transfer driver is carried out by the data transfer host system. (col.9, lines 1-25)

As per claim 24, Larky discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col.4, lines 26-44)
- a downstream USB port; (fig.1,106)
- a memory (fig. 1, 122) connected to both the first processor and a second processor external to the USB host via a standard microprocessor bus interface. (fig.2, 118), (col.4, lines 1-25)
- wherein a first area of the memory with first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer. (col.7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

As per claim 25, Larky discloses a hub (fig.1, 130) connected to the downstream USB port so that multiple devices can be connected to the system.

As per claims 27 and 55, Larky discloses a third area of the memory with a third predetermined format is used for reporting device connection, enumeration and removal to the second processor. (col.4, lines 26-44), (col.5, lines 15-48)

As per claim 28, Larky discloses third area is in a part of the memory that is read-only to the second processor. (fig.1, 122)

As per claims 29 and 56, Larky discloses a fourth area of the memory with a fourth predetermined format is used for sending a USB command to the said USB host. (col.6, lines 5-25)

As per claims 30 and 57, Larky discloses the starting address of each memory area for a transfer is used to identify the transfer. (col.8, lines 19-67)

As per claim 31, Larky discloses the second processor allocates the size of a memory area for a transfer to fit the need of the transfer. (col.8, lines 19-67), (col.9, lines 1-25)

As per claim 32, Larky discloses the second processor allocates the number of the said areas to fit the need of a transfer. (col.8, lines 19-67)

As per claim 38, Larky discloses second processor writes a transfer request in a said area in the memory and notifies the first processor with an interrupt signal. (col.8, lines 51-67)

As per claim 39, Larky discloses the first processor writes the status or data of a transfer into a said area in the memory and notifies the said second processor with an interrupt signal. (col.8, lines 51-67)

As per claim 40, Larky discloses a single format of the said second area implements isochronous, interrupt and bulk transfers. (col.8, lines 51-67)

As per claim 41, Larky discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col.4, lines 22-44)
- a downstream USB port; (fig.1, 106)
- a memory accessible (fig. 1, 122) by both the first processor (fig.1, 126) and second processor(fig.1, 120) external to the said USB host, via a standard microprocessor bus interface. (fig.1 118)
- wherein the second processor initiates a USB transfer by writing a transfer request, and data to be transferred into a first area in the memory, and wherein the first processor carries out the transfer and writes the status of the transfer, and any transferred data into a second area in the memory. (col.7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

As per claim 42, Larky discloses a hub (fig.1, 130) is connected to the downstream USB port so that multiple devices can be connected to the system.

As per claim 46, Larky discloses the second processor runs an operating system that supports a USB driver and wherein a USB transfer initiated

request by the second processor to USB driver is carried out by the USB host. (col.4, lines 1-44)

As per claim 47, Larky discloses wherein the USB host transmits an interrupt signal to the second processor to notify the second processor that the transfer has been completed. (col.9, lines 9-14)

As per claim 48, Larky discloses wherein the second processor transmits an interrupt signal to the USB host to notify the USB host that the second processor has initiated a USB transfer.(col.8, lines 51-67) , (col.9, lines 4-14)

As per claim 49, Larky discloses a USB host system operationally coupled to a computing system with a main processor, comprising a processor (fig.1,120) that interfaces with the main processor (fig.1, 116) via a communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the processor schedules and completes the request via a USB host controller. (col.4, lines 26-44), and

wherein the main processor and the processor are operationally coupled via a standard microprocessor bus interface. (fig.1, 118)

As per claim 50, Larky discloses the processor returns status (fig.5, 506) and data to the main processor based on a request from the main processor. (col.9, lines 26-47)

As per claim 51, Larky discloses the communication area is a dual port memory (fig.6, 608) with plural registers.

As per claim 52, Larky discloses the main processor may poll the communication area and/or be notified by an interrupt generated by the processor. (col.8, lines 51-64)

As per claim 53, Larky discloses the communication area is divided into a first area with a predefined format for a first type of transfer, and a second area with a second predefined format for a second type of transfer. (col.4, lines 26-44), (col.8, lines 18-64)

As per claim 58, the main processor may allocate the dual port memory areas for a transfer. (col.9, lines 26-48)

As per claim 59, the dual port memory may implement isochronous, interrupt and /or bulk transfers. (col.8, lines 51-67)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

g. As per claims 33, 35-37 and 44-45 Larky fails to discloses starting address are being different, same or fixed location of memory, Larky does teach the configuration data load into the device RAM. (col.8, lines 57-60)

Examiner take Official Notice of the starting address being located in a different part of memory is well known in the art. It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate the starting address being located in a different part of memory into Larky's method so as to increase the flexibility of the system.

Response to Amendment

4. Applicant's arguments filed 4/07/03 have been considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Ellis's reference is lack of communication area directly accessible by both the main processor and the first processor. However, Larky's reference discloses data receive and download into RAM(fig.1, 122) from host and control under controller 126 (processor), (col.7, lines 1-20)

b. In response to applicant's argument that Larky's reference doesn't disclose processors connected to host via a standard micropocessor bus interface. However, Larky discloses host CPU 116 connected to USB interface (fig.1, 118) which interfaces USB 106 so that information can be transferred between host and device 101. (col.4, lines 5-14)

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.*

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

June 12, 2003

RUPAL DHARIA
PRIMARY EXAMINER